Hierarchical Model Order Reduction of Systems under Parameter Variations

ModRed 2013

Magdeburg – 11.-13. December 2013

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Agenda

- Introduction
  - Motivation
  - Hierarchical Systems
- Hierarchical Model Order Reduction of Systems under Parameter Variations
- Sequential Hierarchical Model Order Reduction of Systems under Parameter Variations
- Example

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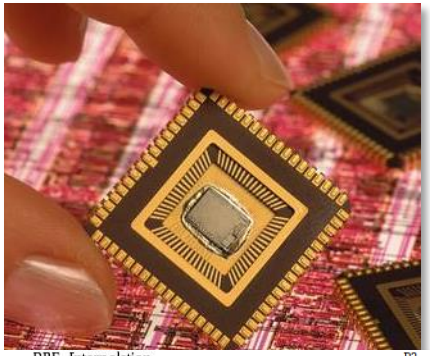
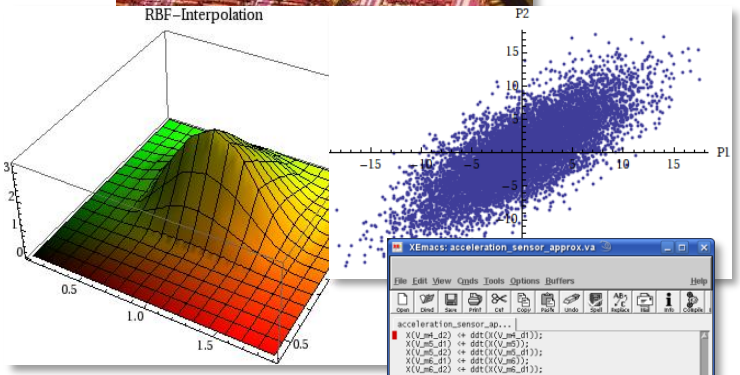
Introduction
Motivation



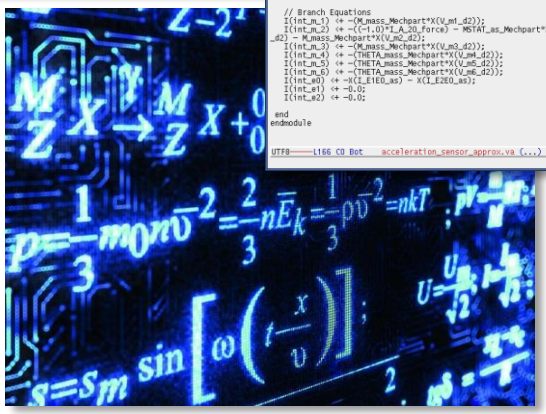


Analog semiconductor devices

- Faster and more powerful
- Trend from micro- to nano-electronics
- Growth of the relative parameter variations during circuit production
- Increasing size of analog circuits

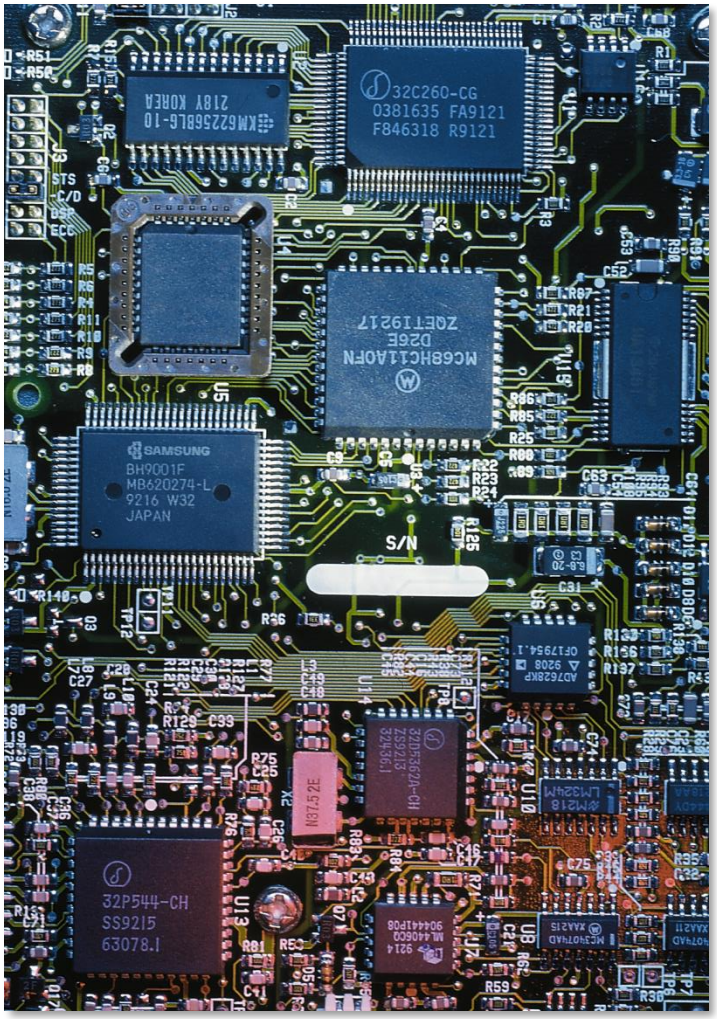
Assist the design of robust circuits to increase the yield of produced circuits

- Generate a reduced (nonlinear) behavioral model taking parameter variations into account to
  - reduce the simulation time
  - increase the insights in the system behavior



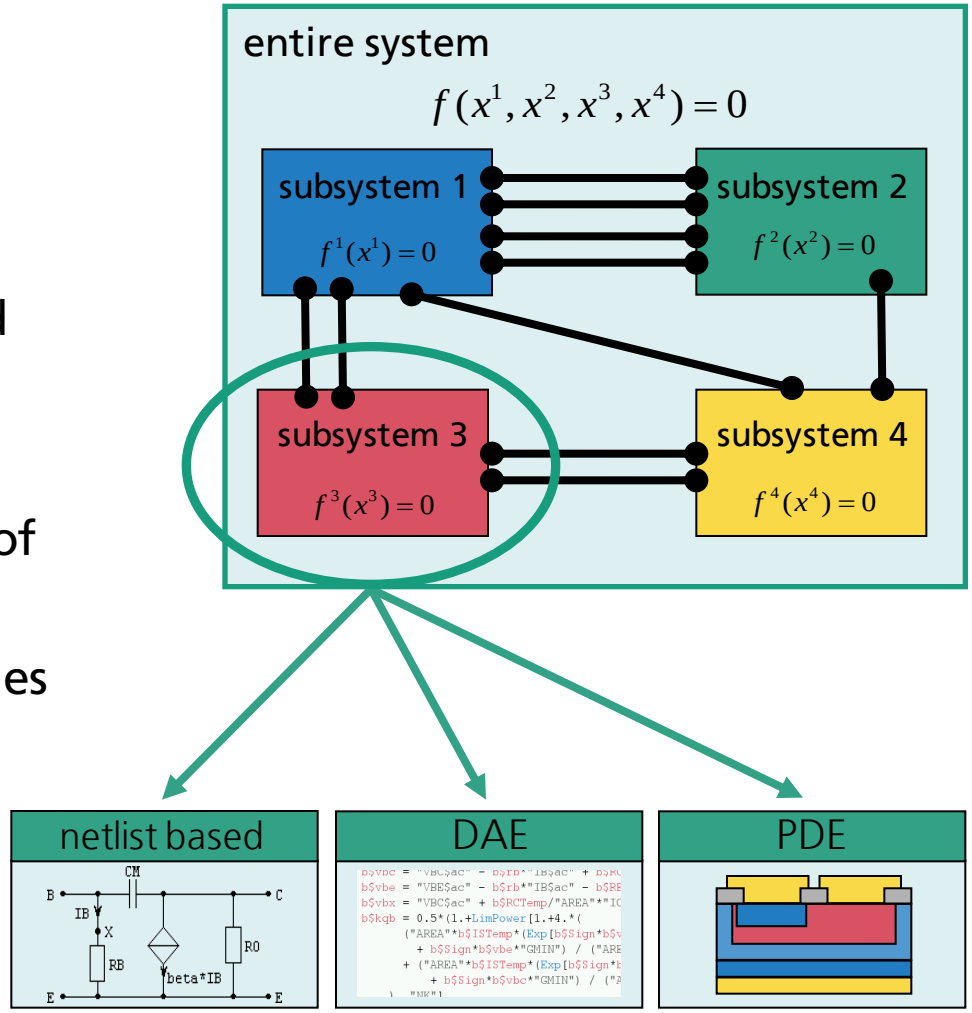
Introduction
Motivation

- Goal
  - Reduced behavioral models to support the design of robust analog circuits under process variations
- Problem
  - Growing size of modern analog circuits
  - MOR needs more and more time
- Idea
  - Use hierarchy of analog circuits for fast MOR



Introduction
Hierarchical Reduction

- **Idea:** Exploitation of hierarchy
  - Reduce subsystems separately
  - Replace subsystems by reduced models
- Advantages
  - Faster and parallel processing of smaller problems
  - Coupling of different techniques
  - Recursive approach possible
    → Level concept
  - Larger nonlinear circuits processable



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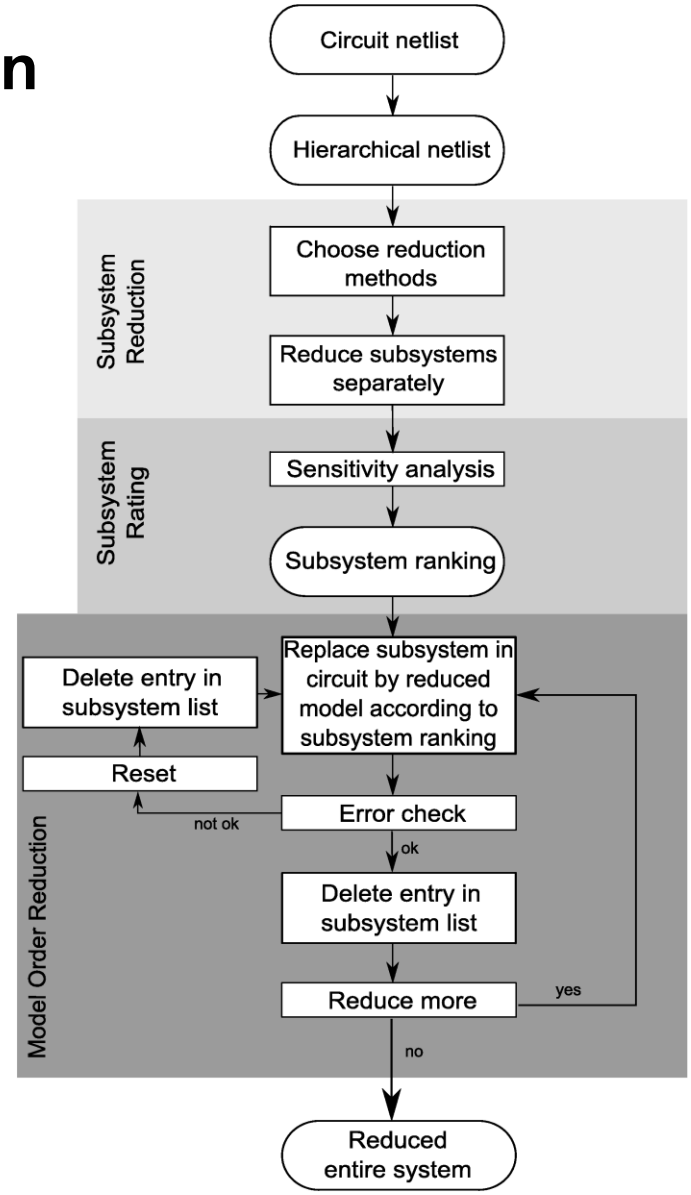
Hierarchical Model Order Reduction

Algorithm Overview

3 Steps

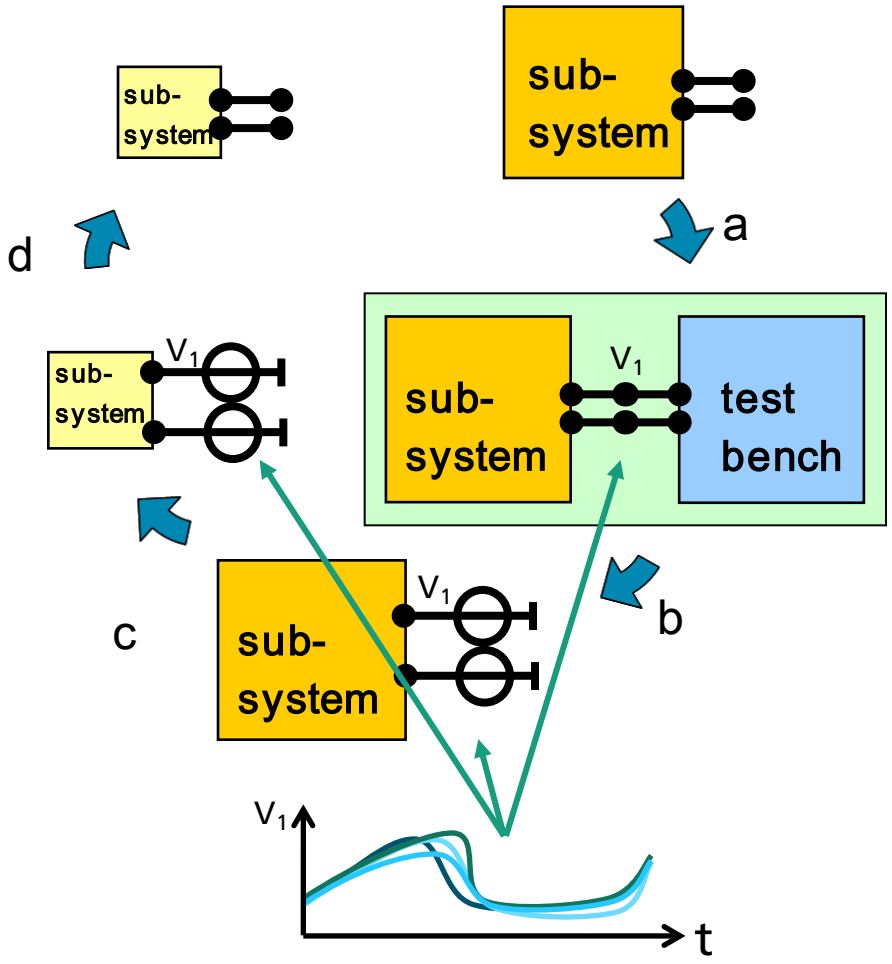
- Choose **reduction** methods for separated **subsystems**
- Compute several reduced models for each subsystem
- **Rate** the reduced subsystems
- **Recombine** the reduced subsystems to a reduced overall system
- Guarantee the accuracy by checking the accumulated error after each replacement



Hierarchical Model Order Reduction

Subsystem Reduction (step 1)

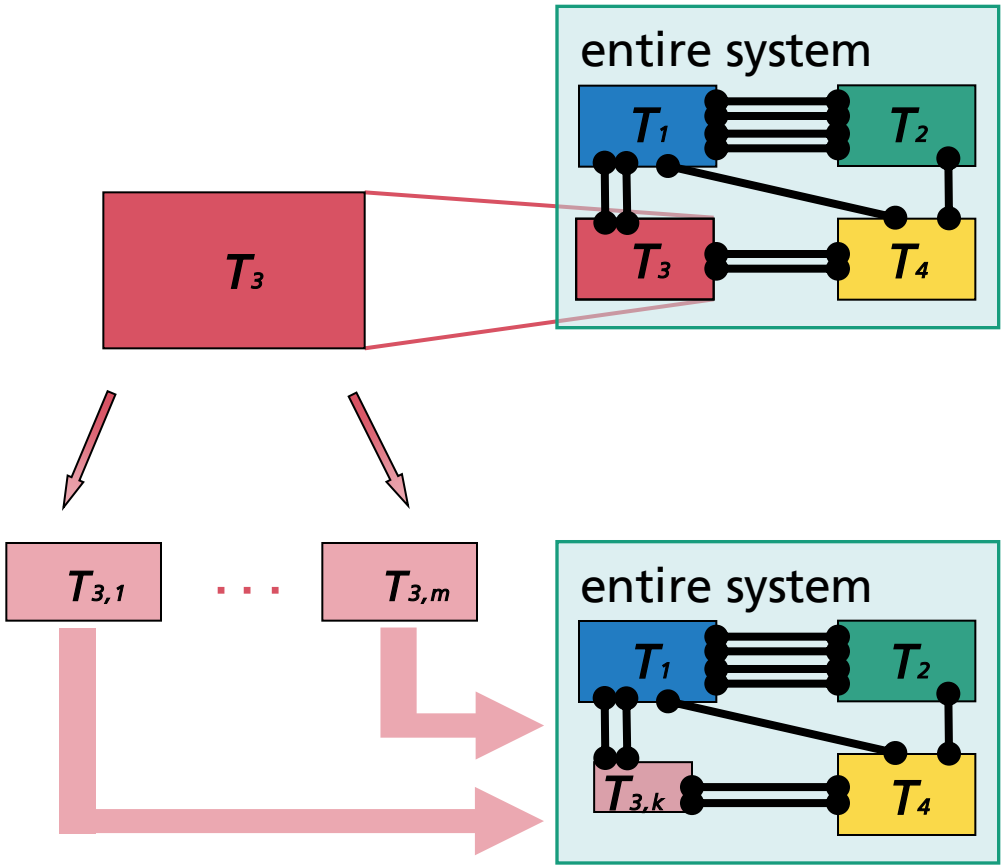
- Simulate subsystem in test bench (a), record voltage potentials at subsystem terminals
- Connect subsystem terminals to voltage sources (b)
- Setup of describing system of equations and reduction (c)
- Removal of sources yields reduced subsystem (d)



Hierarchical Model Order Reduction

Subsystem Reduction (step 1)

- How much can we reduce the subsystem such that the overall system's approximation error limit is fulfilled?
- For each subsystem, produce several reduced versions and rate them in a next step



Hierarchical Model Order Reduction

Subsystem Rating (step 2)

Definition Subsystem rating

- electrical circuit

$$\sum = (\{T_i \,|\, i = 1, \ldots, m\}, S)$$

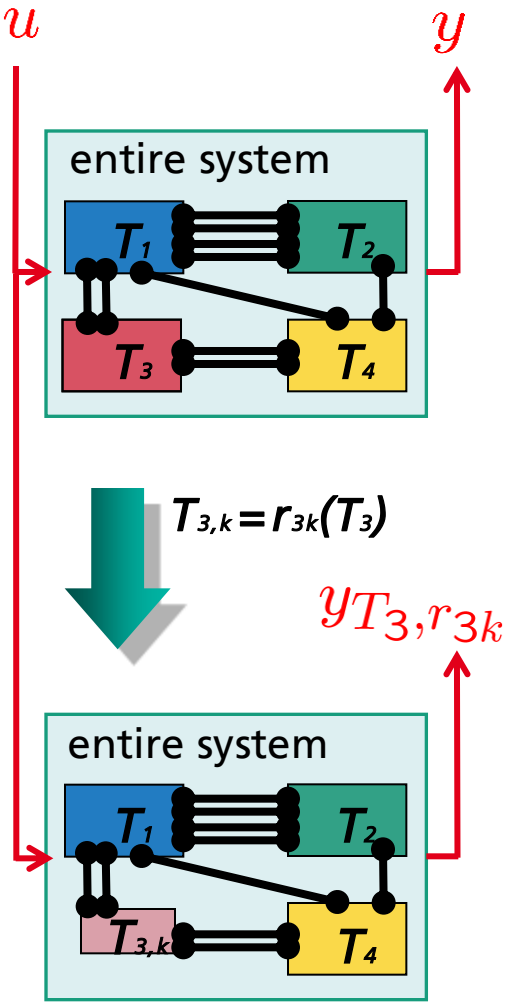
- reduction information r_{ij}, e.g.

r_{ij} = "symbolic reduction, 10%" or

r_{ij} = "Arnoldi, 5 steps"

- error function E
- rating of T_i:

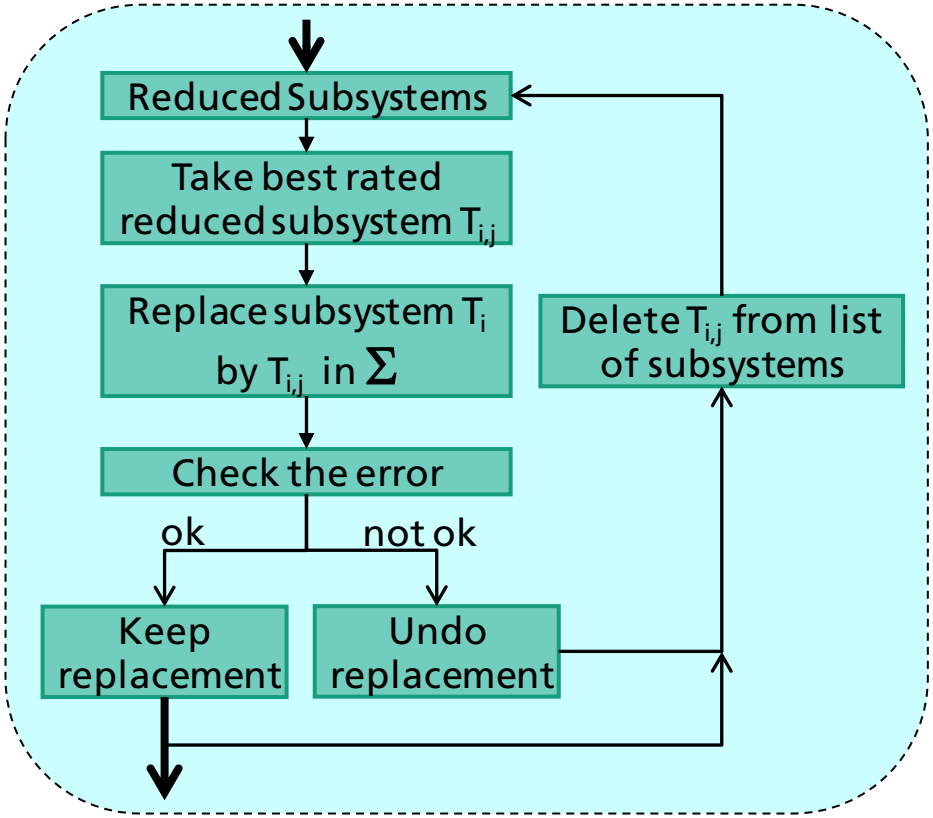
$$s_{T_i} = \left(\left(r_{i1}, E(y, y_{T_i, r_{i1}}) \right), \ldots, \left(r_{im_T}, E(y, y_{T_i, r_{im_T}}) \right) \right)$$



Hierarchical Model Order Reduction

Subsystem Recombination (step 3)

- In each step of the iteration
  - Take the best rated reduced subsystem $T_{i,j}$
  - Replace the respective subsystem T_i by the corresponding model $T_{i,j}$
  - Check the accumulated error of the overall system
  - Keep the subsystem $T_{i,j}$ if and only if the error limit is not exceeded
  - Delete the checked subsystem $T_{i,j}$ from the list of reduced subsystems

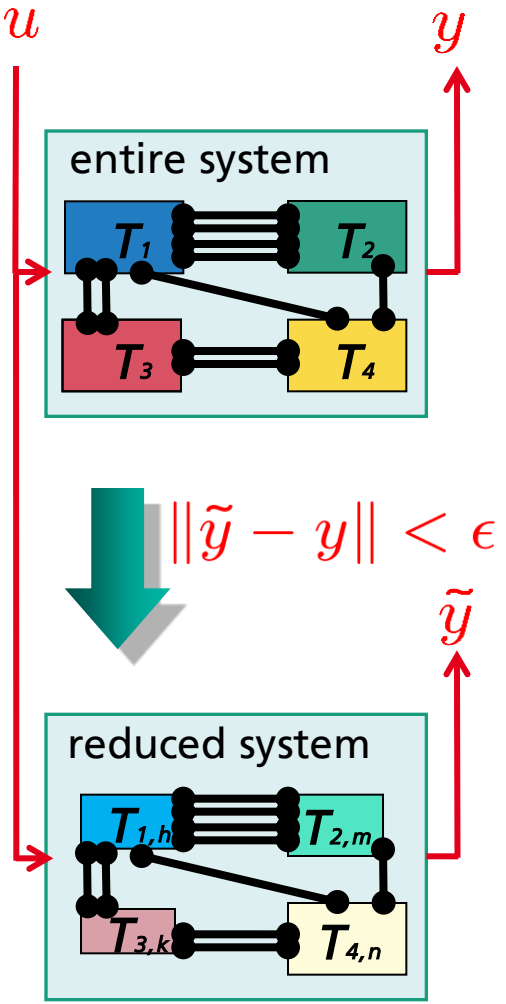


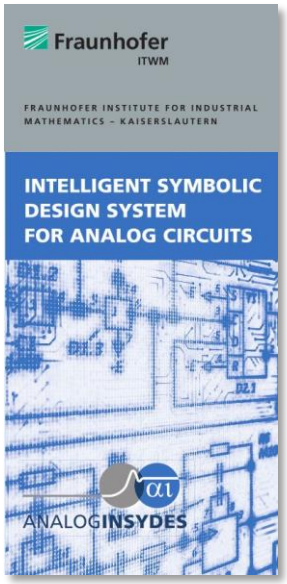
Hierarchical Model Order Reduction

Result

- Reduced overall system containing reduced subsystems
- Symbolic circuit equations and subcircuit structure is preserved
- Predefined error limit is fulfilled
- Implementation of the described methods as an add-on *HierMOR* for the software tool

  Analog Insydes



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<< AnalogInsydes`
<< AnalogInsydes`HierMOR`
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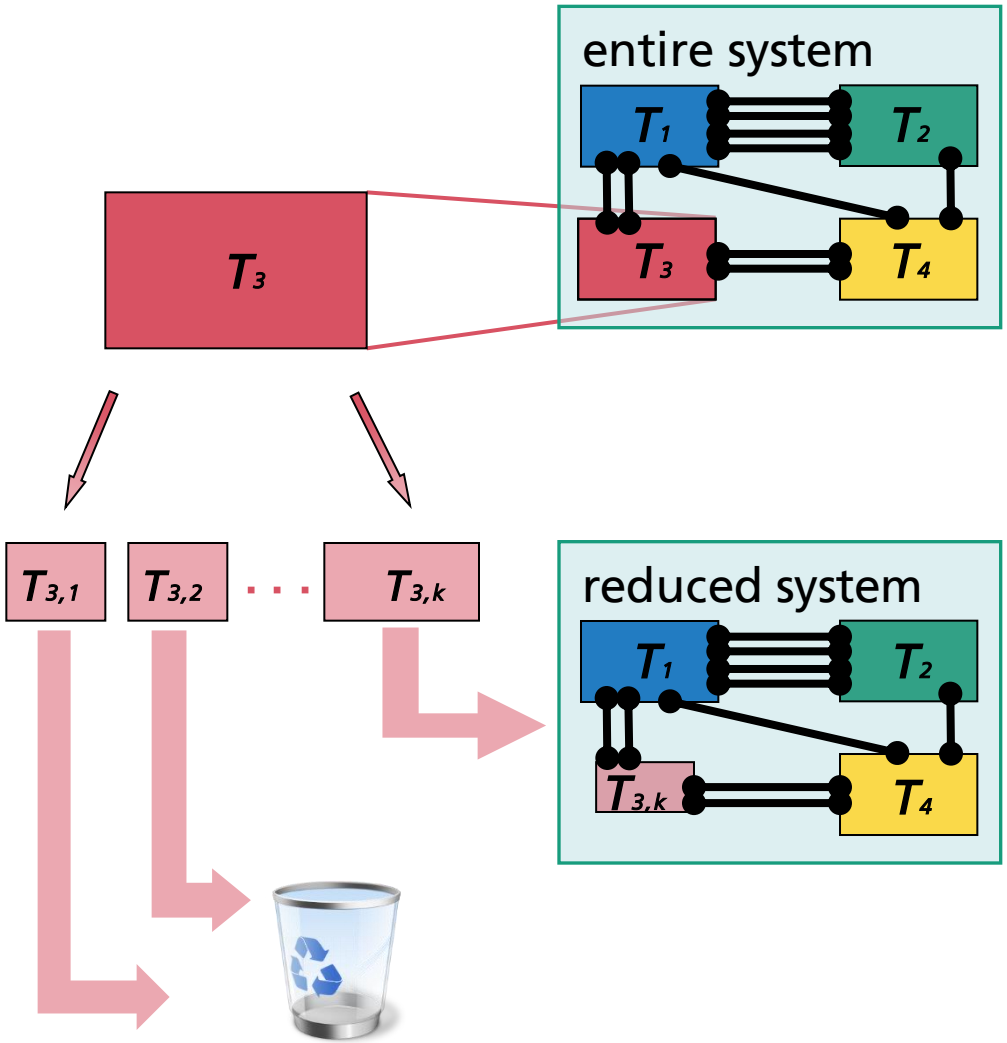
Sequential Hierarchical Model Order Reduction

Motivation

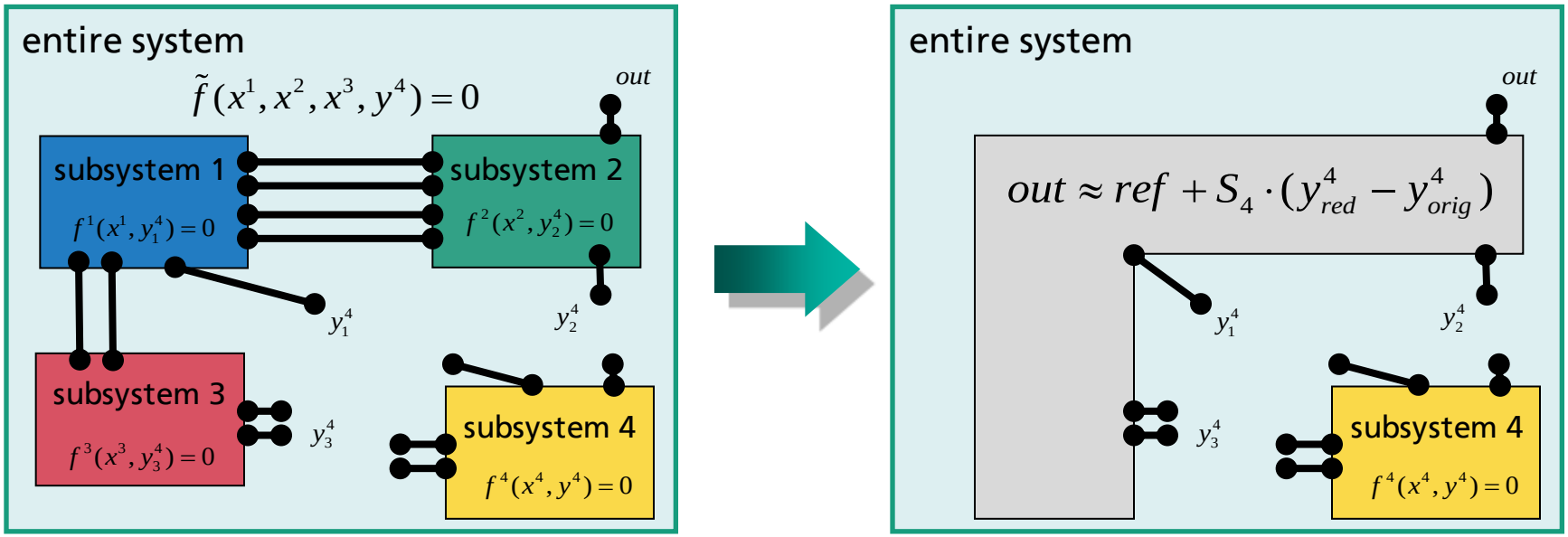
- The presented algorithm generates a high number of reduced subsystems that are not used
- Decide on the fly how much we can reduce the single subsystems
- We need to know how the reduction of a subsystem influences the overall system's output



Sequential Hierarchical Model Order Reduction

Idea

- Reduce subsystem 4 using S_4 such that $error(ref + S_4 \cdot (y^4_{red} - y^4_{orig}), ref) < \varepsilon$
- Check if error bound is exceeded $error(out, ref) < \varepsilon$
- Update ε or reduce next subsystem



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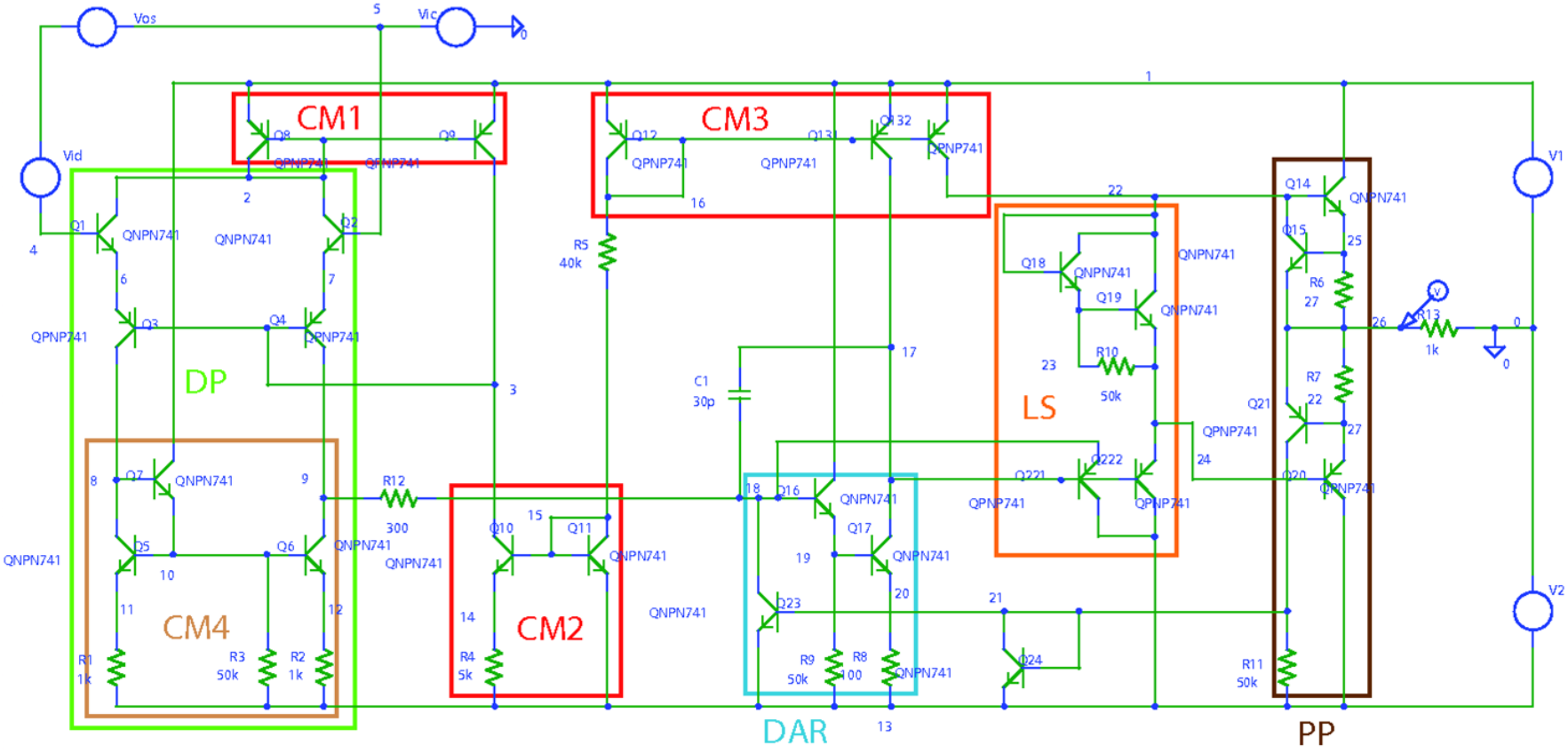
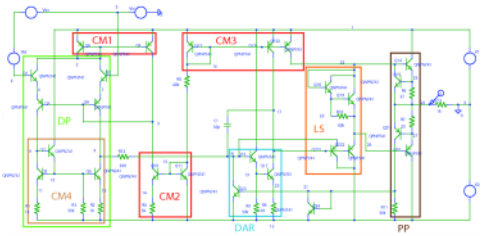
Example

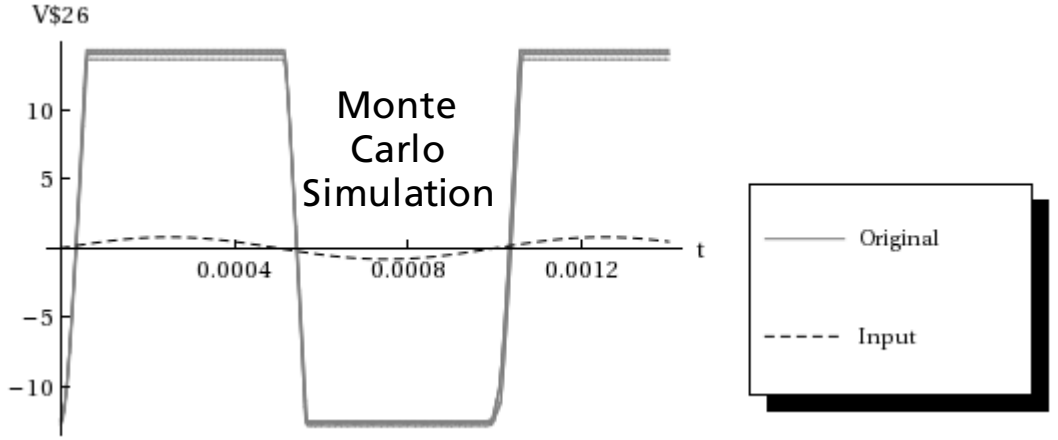
Operational Amplifier 741



Example
Hierarchical Approach



- 26 BJTs, 13 resistors and one capacitor
- Divided into 7 sub blocks
- 1KHz sine as input in the interval [0s, 1.2μs]
- Normal distributed transistor areas, resistor and capacitor values with standard deviations of 1-5%
- Reduction of the transient nonlinear model
- Relative error function
- Error bound 0.3



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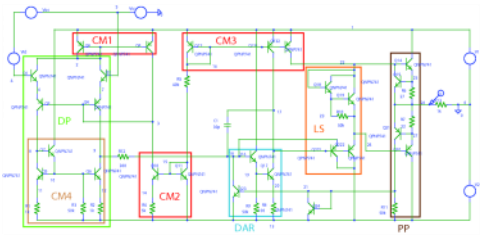
Hierarchical Approach



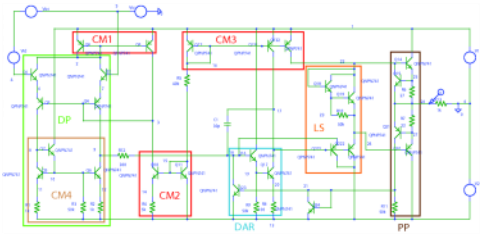
- Final results

	Original system	
Equations	215	
Terms	{1050, 386}	
Simulation time	5.01s	
Reduction	hierarchical method	non hierarchical method
Time	15306s	37750.4s
Equations	112	215
Terms	{494, 290}	{1031, 532}
Rearrange		
Time	7.06s	11.21s
Equations	60	97
Terms	{458, 708}	{828, 541}
Simulation time	1.50s	2.11s
Relative error	0.211873	0.10474

2 times faster

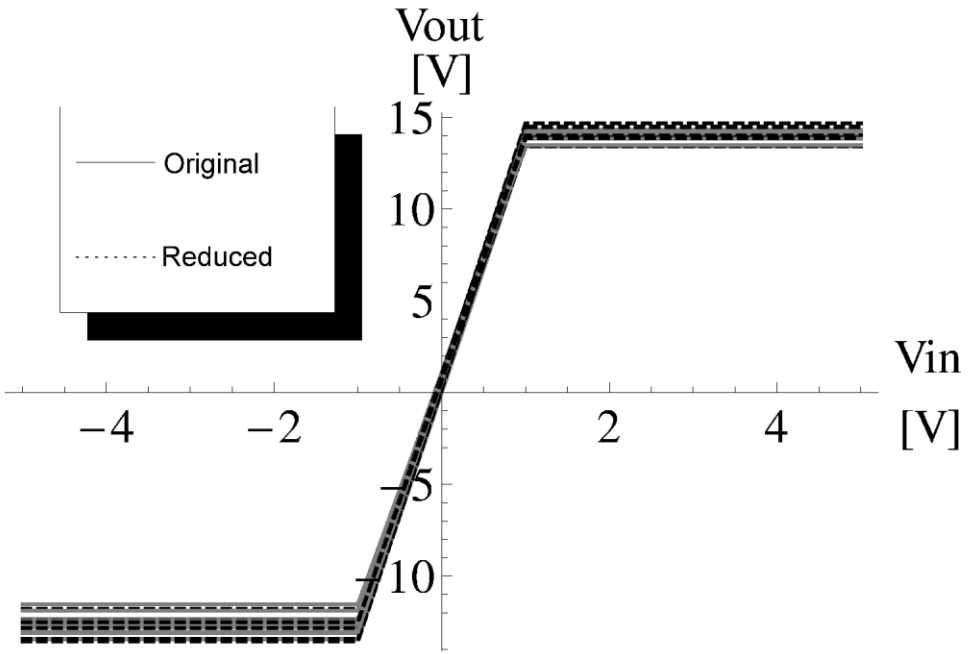
More reduced

Example
Sequential Hierarchical Approach



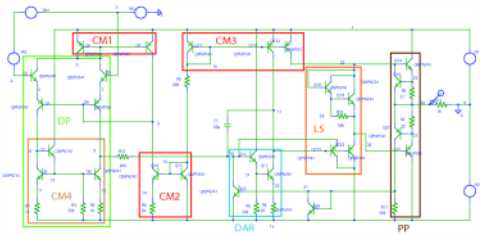
- Approximation of the static behavior
- 4 operating points (–5*V*, –1*V*, 1*V*, 5*V*)
- Statistical error function with 0.3 as error bound

Monte Carlo Simulation



Example

Sequential Hierarchical Approach



- Final results

	Original system		
Equations	229		
Terms	{912, 188}		
Simulation time	8.36s		
Reduction	sequential hier. method	hierarchical method	non hierarchical method
Time	798.47s	26289.30s	47791.25s
Equations	146	135	229
Terms	{585, 164}	{517, 136}	{359, 64}
Umordnen			
Time	4.28s	3.01s	2.36s
Equations	22	23	31
Terms	{405, 316}	{274, 248}	{96, 62}
Simulation time	0.63s	0.76s	0.21s
Statistical error	0.034	0.11	0.27

Further acceler-ation

Less reduced

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M. Hauser, P. Lang: *Sequential Hierarchical Model-order Reduction for Robust Design of Parameter-varying Systems*, 13. GMM/ITG-Fachtagung Analog 2013, Entwicklung von Analogschaltungen mit CAE-Methoden, Aachen (2013), ITG-Fachbericht 239, ISBN 978-3-8007-3467-2, VDE VERLAG GMBH, Berlin Offenbach

M. Hauser, C. Salzig: *Hierarchical Model-order Reduction for Robust Design of Parameter-varying Systems*, International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), September 2012, Sevilla, Spain

This work was funded by BMBF

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