O-MOORE-NICE!
New methodologies and algorithms
for design and simulation of analog integrated circuits

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Introduction

In the EU-project O-MOORE-NICE![1] major achievements have been obtained in dedicated computational methods for integrated circuit (IC) design: Model Order Reduction (MOR) techniques for linear and nonlinear problems; behavioral modeling; and multi-objective optimization, and response surface modeling. On all these topics, not only a lot of publications have appeared in journals and conference proceedings, but also lectures were given at industry and at universities. Furthermore, prototype software is in use at both NXP and the academic partners. Among the successes are the development of nonlinear phase macromodeling techniques for analysis of oscillators, a new approach of nonlinear MOR via table interpolation and response surface modeling, and algorithms for the solution of large networks arising in Electro-Static Discharge analysis.

O-MOORE-NICE! [Operational MOdel Order REduction for Nanoscale IC Electronics][2] was a FP6 Marie Curie Action program in which Transfer of Knowledge (ToK) on computational methods for IC design between three universities was exchanged with industry: Chemnitz University of Technology

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[2]http://www.tu-chemnitz.de/mathematik/industrie_technik/projekte/omoorenice/index.php?lang=en

Figure 1: Example of an integrated circuit in a package.

(CUT), University of Antwerp (UNA), Eindhoven University of Technology (TUE) and NXP Semiconductors, Eindhoven (NXP). The EU-Project started on Feb. 1, 2007 and reached its completion on Jan. 31, 2010. Three academic fellows stayed at NXP for two years, while the NXP fellow alternated periods at NXP with visiting the academic partners for some periods. This formed the basis pattern for ToK. It guaranteed much interaction between the fellows and also between the host organization and the academic partners. The secondment periods were part of the funding by the EU program.

Status at the start
Simulation plays a major role in computer-aided design of integrated circuits (ICs). Mathematical models describe the dynamical processes and interactions of electrical devices. Verification of a circuit's behaviour by means of solving these model equations in time and frequency domain is a mandatory task in the design process. The structures' sizes are decreasing, the packing density gets higher and so do the driving frequencies (up into the GHz area). This results in chips (e.g., Fig. 1) used for modern mobile devices, that typically have an FM radio, Bluetooth, and GPS on one chip. The chips can be combined with functionality for cameras, for checking a person's identification, for contacting bank accounts, automobile cruise and climate control, or television set top. It combines parts for analogue signals with parts for digital signals. To design such products means that simulation has to deal with problems that, on the contrary, become larger in size. It requires using refined models for the more detailed physics (nonlinear and high frequency effects) and after layouting secondary, parasitic effects have to be taken into account. The very high dimensional problems that emerge in this way may be solvable with the help of computer algebra in an unreasonable amount of time only. Clearly, this conflicts with the short time-to-market demands in industry. Model Order Reduction (MOR) presents a way out of this dilemma. Redundancies are resolved, less relevant quantities are replaced by the most significant ones. The input-output behaviour of a building block maintains its characteristics, but its size is reduced. Solving lower dimensional problems one can obtain statements on the circuit's performance more quickly. Knowledge and experience in this field of computational science is scattered across european universities and companies.
Chemnitz University of Technology (Prof. Peter Benner) contributed knowledge on Model Order Reduction, University of Antwerp (Prof. Tom Dhaene; now at Ghent University) contributed experience on techniques for parameterized Response Surface Modeling, Eindhoven University of Technology (Prof. Wil Schilders) brought in Behavioral Modeling. NXP Semiconductors (Dr. Jan ter Maten and
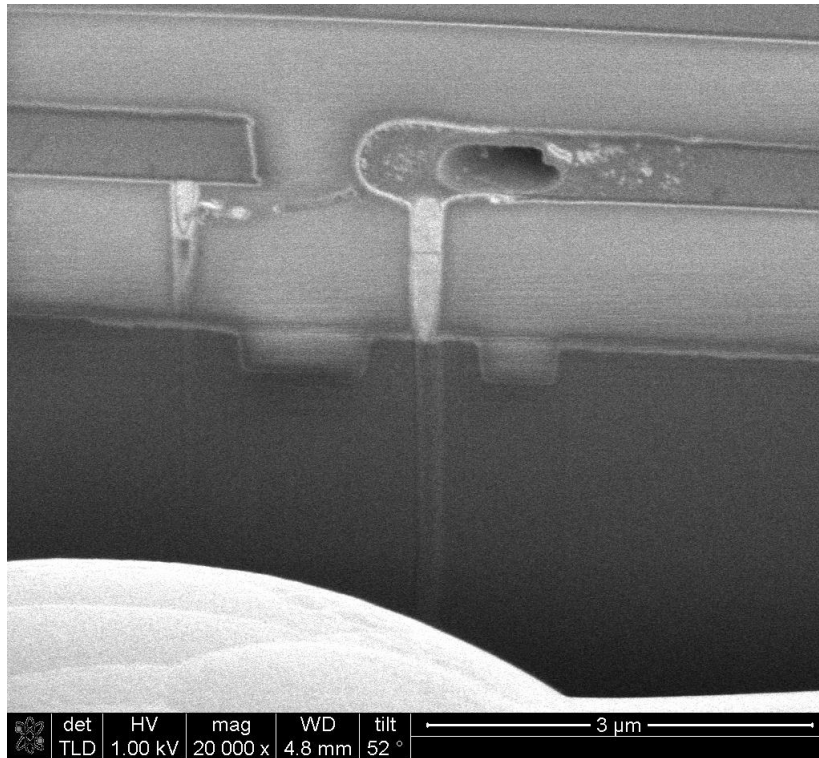
Figure 2: Unwanted elecro-static discharge: close-up of interconnect that was damaged by a current density higher than the metal's capacity.

Ir. Marcel Sevat) contributed the experience in simulating designs.

Four postdocs were recruited: Dr. Michael Striebel (CUT), Dr. Luciano De Tommasi (UNA), Dr. Davit Harutyunyan (TUE) and Dr. Joost Rommes (NXP). The team started to collect problems and noted that methods had to be further developed. MOR needed enhancements to cover nonlinearity, to cover input-output between many terminals. Optimization had to deal with many objectives and constraints. Behavioral modeling had to deal with parameterization.

Scientific and technological highlight I: Model Order Reduction

As a result, breakthrough achievements have been obtained in MOR for linear and nonlinear problems, behavioral modeling and multi-objective optimization, and response surface modeling. On all these topics, not only publications have appeared in journals and conference proceedings, but also lectures were given and prototype software is in use at both NXP and the academic partners.

For the simulation of large RC-systems with many terminals a novel approach has been developed which allows partitioning of the structure into subsystems. These subsystems allow further reduction by reducing the number of nodes that do not connect to their environment. Solving a special eigenvalue problem, which results in a system of minimum dimension, yields the identification of the nodes. The approach is currently used at NXP to verify performance of designs after parasitics extraction of layouts. Also electro-static discharge paths are now simulated orders faster than before (Figure 2). The hard problem to derive accurate and efficient MOR for nonlinear systems started with a thorough study of techniques available at the beginning of the project. Methods were improved but

were still subject to changes in input-output behaviour. Recently a table interpolation process was developed that combined the wanted features: accurate, fast, allow for re-use.

Scientific and technological highlight II: Behavioral modeling
Another important aspect of the project was to investigate behavioral modeling of on-chip oscillators. In the design process, floor planning, i.e., determining the locations of the functional blocks, is one of the most challenging tasks (Figure 3). Features on modern RF chips for mobile devices are implemented with Voltage Controlled Oscillators (VCOs), that are designed to oscillate at certain different frequencies. In the ideal case, the oscillators operate independently, i.e., they are not perturbed by each other or any signal other than their input signal. Practically speaking, however, the oscillators are influenced by unintended (parasitic) signals coming from other blocks (such as Power Amplifiers) or from other oscillators, via for instance (unintended) inductive coupling through the substrate. A possibly undesired consequence of the perturbation is that the oscillators lock to a frequency different than designed for, or show pulling, in which case the oscillators are perturbed from their free running orbit without locking. Nowadays oscillators are running at a very high frequency range ($>$1GHz) and hence full transient simulation would not permit to do fast analysis of coupled oscillators, because it would require very small time steps to achieve accuracy. To reduce the computational time of full transient simulation in the project we considered a behavioral modeling approach where the response of an oscillator is determined by a single scalar equation for the phase shift. The essence of the method is to do only once an expensive periodic-steady-state analysis for an oscillator. Next the response of the whole system can easily be determined for various types of coupling, e.g., oscillator-oscillator and oscillator-balun coupling. This method was used by NXP to efficiently and accurately identify right locations of two inductively coupled on-chip oscillators in order to minimize unwanted coupling between them.

Scientific and technological highlights III: Response Surface Modeling
Research activities on Response Surface Modeling (RSM) concerned the behavioral modeling of RF building blocks (a.o. Low Noise Amplifier). The work concentrated on both forward and reverse modeling problems. Typical applications of a forward model include what-if analysis, optimization and sensitivity analysis. On the other hand, reverse modeling concerns multi-objective optimization to explore relevant trade-offs between circuit performances. The most complete and natural way to figure out such trade-offs is the computation of Pareto fronts. Forward models were used in combination with multi-objective optimization to speed-up the generation of reverse models. Software improvements on NBI (Normal Boundary Intersection) and SPEA2 were developed with NXP. Finally, the various experiments lead to further improvements of the SUMO toolbox developed by Surrogate Modeling Lab[3] at Ghent University (formerly at Univ. of Antwerp). Results were handed to NXP Research.
Recently the obtained knowledge facilitated development of a new methodology for semi-automated IP Designs via parameterized layouts and optimization with NXP Research and is currently used at NXP sites in France and in Austria.

Transfer of Knowledge
Being most of the time at the same place there was intensive interaction between the fellows for the mathematical aspects. They exploited their contacts with specialists at academia. They interacted with IC design experts at NXP for the electrical aspects: first the practical problem, e.g., oscillator pulling, had to be understood, which requires interaction with designers. Next a mathematical formulation has

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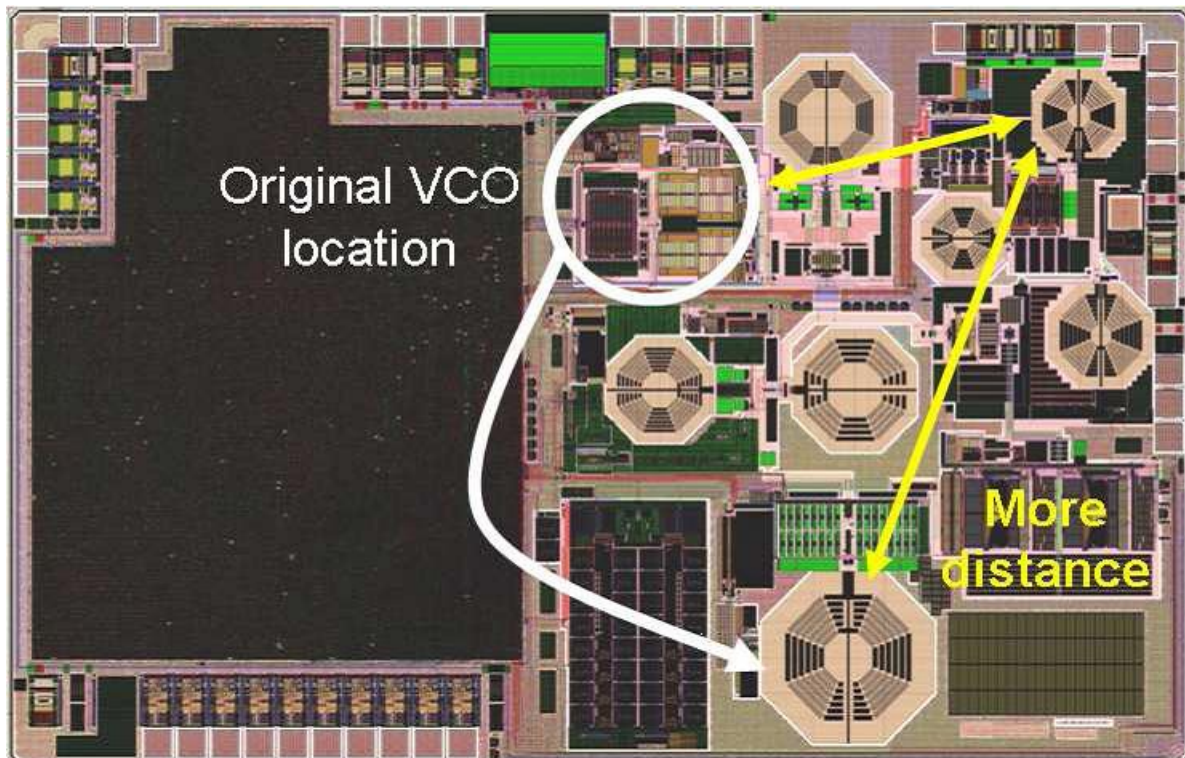
[3]http://sumo.intec.ugent.be/

Figure 3: Floor plan with relocation option that was considered after nonlinear phase noise analysis showed an intolerable pulling due to unintended coupling. Additionally, shielding was used to limit coupling effects even further.

to be made, after which the problem could be solved mathematically. Finally, the solution had to be transferred back to the problem owner, i.e., the designer. These three phases were typically iterated several times, a process which was enabled by all fellows being present at the host organization for nearly two years. This resulted in a transfer of broad knowledge on applications and mathematical solution methods between the fellows, the host, and the partners.

The way of working, presentation of intermediate and final outcomes, the prioritization during the various project steps were practical learning points. In addition the presentation to and interaction with management and engineers in electronics industry (IC designers) meant crossing interdisciplinary borders.

A continuous reading group among the fellows, MSc- and PhD-students and NXP staff served the purpose of scanning recent literature and distributing the knowledge obtained among them. The fellows have trained quite a number of PhD-students [TUE (2), Jacobs Univ. Bremen, Bergische Universiät Wuppertal, Politehnic Univ. Bucharest, TU Braunschweig, CUT] and MSc-students [KTH Stockholm, TUE (2), Univ. of Toulouse] during the project.

All fellows learned new methods and numerical techniques from external experts, in the context of 12 meetings of NXP's Numerical Mathematics Working Party (NMWP) during the project period. In the morning two 45-minutes presentations were given, in the afternoon more detailed discussions were set up. All fellows gave a presentation at one or more meetings of the NMWP. The external visitors did come from MAGWEL (Leuven), Utrecht University, Univ. of Bielefeld, KU Leuven/Kortrijk,

TU Delft, Tilburg Univ, Ghent University, CUT, Univ. of Cologne, Silvaco Technology Centre (Cambridge), DOW Benelux (Terneuzen), Rice Univ. (Houston, TX), Jacobs Univ. (Bremen), Univ. of Groningen. The meetings were also attended by colleagues from TUE, TU Delft and Bergische Universität Wuppertal.

Dissemination

All fellows gave lectures on their topic at the SyreNe & O-MOORE-NICE! Workshop on Model Reduction for Circuit Simulation at TU Hamburg on 30/31-10-2008 [51 participants], at the O-MOORE-NICE! Workshop held at TUE on 30 January 2009 and at the Final Workshop at TUE on Jan. 22, 2010. Several PhD students and staff from TUE (Depts of Mathematics and Electronics) attended these last workshops.

At the technical meetings at CUT (18-01-2008) and at UNA (29-08-2008), the public part was attended by local staff.

Results were presented at the MOR Symposium at TUE on 23-11-2007; at SCEE-2008[4] (Scientific Computing in Electronic Engineering) in Espoo, Finland; at the IEEE Conference on Computational Science and Engineering in Rio De Janeiro (14-07-2008); at IEEE SPI-2008 (Signal Propagation on Interconnects, Hannover); at IEEE International Conference on Microwaves, Radar & Wireless Communications (MIKON 2008, Kraków, Poland); at IEEE World Congress on Computational Intelligence (WCCI 2008, Hong Kong); at the Workshop on Optimization and Inverse Problems in Electromagnetism (OIPE 2008, Ilmenau); at the SIAM Conference on Computational Science and Engineering (CSE) 2009 in Miami, Florida.

At ECMI-2008[5], London, a mini-symposium was organized jointly with fellows from the Symteco ToK project (between STM-Catania and Fraunhofer ITWM Kaiserlautern). Collaboration with the MCA-RTN COMSON[6] project resulted in presentations at the COMSON MOMINE-2008 Summer School on Sicily (June 2008), combined with a meeting with the Symteco ToK project at STM-Catania. Results were also presented at the COMSON Autumn School[7] on Future Developments in Model Order Reduction at Terschelling, the Netherlands (21/25-09-2009) [84 participants] and at the SIAM Conference on Applied Linear Algebra (24/27-10-2009) in Monterey, CA.

Visits were made to Dublin City Univ, MATHEON (Berlin), Hamilton Institute in Maynooth, Imperial College London. Invited talks will be given at the ASIM Workshop[8] in Ulm (04/05-03-2010) and at SCEE-2010[9] in Toulouse (19/25-09-2010).

Epilogue

After the project end Davit Harutyunyan found employment at KNMI - Royal Netherlands Meteorological Institute, Luciano De Tommasi at ECN - Energy Research Centre of the Netherlands, and Michael Striebel at Bergische Universität Wuppertal, Germany. Joost Rommes has a permanent position at NXP Semiconductors in Eindhoven. For all university fellows the knowledge obtained in O-MOORE-NICE is beneficial in their new environments.

The project has strengthened the contacts between NXP and its academic partners.

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[4] `http://radio.tkk.fi/en/conferences/scee2008/`

[5] `http://www.ecmi2008.org/`

[6] See also ECMI Newsletter 42, `http://www.mafy.lut.fi/EcmiNL/issues.php?issueNumber=42`

[7] `http://www.win.tue.nl/casa/meetings/special/mor09/`

[8] `http://www.hs-ulm.de/Institut/IFS/Veranstaltungen/_/_root//docs/institute/ifs/veranstaltungskalender/_veranstaltungen/1000304_ASIM/`

[9] `http://sites.onera.fr/SCEE2010/`

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3. D. Harutyunyan, J. Rommes, E.J.W. ter Maten, W.H.A. Schilders: *Simulation of mutually coupled oscillators using nonlinear phase macromodels*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 28, Issue 10, pp. 1456–1466, 2009.

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5. M. Striebel, J. Rommes: *Model order reduction of nonlinear systems: status, open issues, and applications*, Chemnitz Scientific Computing Preprints CSC 08-07, 2008.

For an extensive list of references see: `http://www.tu-chemnitz.de/mathematik/industrie_technik/projekte/omoorenice/index.php?lang=en`